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EXAMINER
MCLEAN-MAYO, KIMBERLY N

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 02/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/667,050	BOGIN ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,9 and 12-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,9 and 12-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The enclosed detailed action is in response to the Amendment submitted on November 25, 2002.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8-9 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (USPN: 6,477,623) in view of Alpert et al. (USPN: 5,802,605).

Regarding claim 8, Jeddeloh discloses using a conversion table (Figure 2, Reference 202) to translate a first address (untranslated address from the graphics controller) from a graphics controller (Figure 2, Reference 140) to a second address (translated first address) to a memory (C 6, L 17-24, L 36-50); and using the conversion table to translate a third address (untranslated address from the bus controller) from a bus controller (Figure 2, Reference 130) to a fourth address (translated third address) to the memory (C 6, L 17-24, L 36-50). Jeddeloh does not disclose the second address having a greater number of bits than the first address and the fourth address having a greater number of bits than the third address. However, Alpert teaches the concept of using a conversion table (page table) to translate an initial address to a translated address wherein the translated address has a greater number of bits than the initial address (C 3, L 36-40; C 4, L 33-40; C 7, L 32-41; C 8, L 12-50). This feature taught by Alpert expands the

addressing capability of an architecture with a limited addressing range, such as the system taught by Jeddeloh, by mapping/translating the virtual/linear addresses to larger physical addresses. The width of the physical address is extended thereby allowing the system to access memory beyond its capabilities based upon the width of the virtual/linear address. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings of Alpert with the teachings of Jeddeloh for the desirable purpose of expanding the addressing capability of a system by allowing the system to access a larger amount of physical memory and thereby improve the performance of the system.

Regarding claim 9, the system taught by Jeddeloh and Alpert disclose the conversion table to translate the third address including a translation lookaside buffer (Jeddeloh – C 6, L 25-35).

Regarding claims 12-14, Jeddeloh and Alpert disclose the conversion table including comparing a first portion (virtual/linear address excluding the offset) of the third address (virtual/linear address) with entries in a first table and if the first portion matches a particular one of the entries in the first table, combining a value (physical page number/address) associated with the particular one with a second portion (offset) of the third address to form the fourth address (physical address) (Figure 3, References 310, 312; C 7, L 9-18 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses (C 6, L 28-30) and thus TLBs function such that the virtual/linear address, [excluding the offset], is compared to the addresses in the TLB and when a match is found, a physical address is formed by combining the physical page number [translated address] with the offset of the virtual/linear address and

thus it is evident that these steps are performed when performing steps 310 and 312 in Figure 3), and if the first portion does not match any of the entries in the first table, referring to a second table (comprehensive table) to translate the third address (Jeddeloh; C 6, L 30-34; C 7, L 12-15), wherein the comparing includes comparing the first portion of the third address with entries in the first table (GART table) in an input-output controller (Figure 2, Reference 102) and wherein the referring to the second table includes referring to the second table (comprehensive table) in main memory (system memory)(C 6, L 30-34; C 7, L 12-15).

4. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (USPN: 6,477,623) in view of Dixit (USPN: 5,574,877).

Regarding claim 19, Jeddeloh discloses a processor (Figure 1, Reference 116); a memory (Figure 1, Reference 104); a graphics controller (Figure 1, Reference 140); a bus controller (Figure 1, Reference 118); an input-output controller coupled to the processor, memory, graphics controller and bus controller (Figure 2, input-output controller is comprised of References 122, 124, 130, 202, 126, and 204), the input-output controller including a translation lookaside buffer (TLB)(Figure 2, Reference 202 -Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses [C 6, L 28-30]); control logic coupled to the translation lookaside buffer (hardware/software responsible for controlling Reference 202); wherein the control logic is to compare a first portion (virtual/linear address excluding the offset) of a first initial address (virtual/linear address) from the bus controller (via Reference 130) (C 6, L 36-50) with entries in the translation lookaside buffer and if a first matching entry is found, combining a first value (physical page number/address) associated with the first matching entry

with a second portion (offset) of the first initial address to form a first translated address (physical address) (Figure 3, References 310, 312; C 7, L 9-18 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses (C 6, L 28-30) and thus TLBs function such that a virtual/linear address, [excluding the offset], is compared to the addresses in the TLB and when a match is found, a physical address is formed by combining the physical page number [translated address] with the offset of the virtual/linear address and thus it is evident that these steps are performed when performing steps 310 and 312 in Figure 3); and wherein the control logic is further to compare a first portion of a second initial address from the graphics controller (Figure 2, Reference 140; C 6, L 36-50) with the entries in the translation lookaside buffer and if a second matching entry is found, to combine a second value (physical page/frame number) associated with the second matching entry with a second portion of the second initial address (offset portion) to form a second translated address (physical address) (Figure 3, References 310, 312; C 7, L 9-18 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses (C 6, L 28-30) and thus TLBs function such that the virtual/linear address, [excluding the offset], is compared to the addresses in the TLB and when a match is found, a physical address is formed by combining the physical page number [translated address] with the offset of the virtual/linear address and thus it is evident that these steps are performed when performing steps 310 and 312 in Figure 3. These same steps are performed for each address provided thereto from any of the elements coupled to Reference 124 in Figure 2 for translation). Jeddeloh does not disclose an input register and an output register coupled to the TLB and control logic, wherein the control logic is to compare a first initial address in the input register with the entries in the TLB and a first translated address is held in

the output register and wherein the control logic is to compare a second initial address in the input register with the entries in the TLB and a second translated address is held in the output register. However, Dixit teaches a TLB (Figure 1, comprised of references 12, 14, 16, 20, 22, 24, 28, 30, 31, 32 and 34) coupled to an input register (Figure 18; C 3, L 12-14) and an output register (Figure 1, Reference 26; C 3, L 20) and control logic (software or hardware logic for controlling the operation of the TLB), wherein the control logic is to compare an initial address in the input register with the entries in the TLB and wherein a translated address is held in the output register (C 3, L 9-22). It is well known in the art to store data/addresses in a register for the purpose of reducing jitter and glitches from the signals thereby providing accurate and stable data outputs. Jeddeloh addresses are not disclosed as stored in registers and thus are vulnerable to the effects of glitches and jitter. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to couple Jeddeloh's TLB to an input register and an output register, wherein a first initial address in the input register is compared with the entries in the TLB and a first translated address is held in the output register and wherein a second initial address in the input register is compared with the entries in the TLB and a second translated address is held in the output register for the desirable purpose of stability and accuracy.

Regarding claim 20, Jeddeloh and Dixit disclose the control logic is further configured to access a table (comprehensive table) in memory if the first matching entry is not found (comprehensive table) to translate the third address (Jeddeloh - C 6, L 30-34; C 7, L 12-15), find a third value (physical page/frame number) in the table associated with the first portion of the first initial address, combine the third value with the second portion of the first initial address to form a third

translated address (Jeddeloh - Figure 3, References 310, 312 - the third value and the offset of the first initial address are combined to perform a memory operation and are thus combined to form a physical address) and hold the third translated address in the output register (Dixit - C 3, L 18-22).

Regarding claim 21, Jeddeloh and Dixit disclose the control logic including logic for first and second control flows, wherein the second control flow is to translate an initial graphics controller address and does not access the table (Jeddeloh – C 7, L 9-12; the control logic responsible for translating an address using the GART, when a GART hit occurs) and wherein the first control flow is to translate an initial bus controller address and accesses the table (Jeddeloh – C 7, L 12-15; the control logic responsible for translating an address using the comprehensive table in system memory – when a GART miss occurs).

5. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (USPN: 6,477,623) and Dixit (USPN: 5,574,877) as applied to claim 20 above and further in view of Alpert et al. (USPN: 5,802,605).

Regarding claim 22, Jeddeloh and Dixit disclose the limitation above in claim 20, however, Jeddeloh and Dixit do not disclose the first translated address having more bits than the first initial address and the second translated address having more bits than the second initial address. Alpert teaches the concept of translating an initial address into a translated address (physical address), wherein the translated address has more bits than the initial address (C 3, L 36-40; C 4, L 33-40; C 7, L 32-41; C 8, L 12-50). This feature taught by Alpert expands the addressing

capability of an architecture with a limited addressing range, such as the system taught by Jeddeloh and Dixit, by mapping/translating the virtual/linear addresses to larger physical addresses. The width of the physical address is extended thereby allowing the system to access memory beyond its capabilities based upon the width of the virtual/linear address. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings of Alpert with the teachings of Jeddeloh and Dixit for the desirable purpose of expanding the address capability of a system by allowing the system to access a larger amount of physical memory and thereby improving the performance of the system.

6. Claims 15-18 and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (USPN: 6,477,623) in view of Alpert et al. (USPN: 5,802,605) and Dixit (USPN: 5,574,877).

Regarding claim 15, Jeddeloh discloses an apparatus comprising a translation lookaside buffer (Figure 2, Reference 202 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses [C 6, L 28-30]); control logic coupled to the translation lookaside buffer (hardware/software responsible for controlling Reference 202), wherein the control logic is to compare a first portion (virtual/linear address excluding the offset) of an initial address (virtual/linear address) with entries in the translation lookaside buffer and if a first matching entry is found, to combine a first value (physical page number/address) associated with the matching entry with a second portion (offset) of the initial address to form a first translated address (physical address) (Figure 3, References 310, 312; C 7, L 9-18 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses (C 6, L 28-

30) and thus TLBs function such that a virtual/linear address, [excluding the offset], is compared to the addresses in the TLB and when a match is found, a physical address is formed by combining the physical page number [translated address] with the offset of the virtual/linear address and thus it is evident that these steps are performed when performing steps 310 and 312 in Figure 3). Jeddeloh does not disclose the first value having a greater number of bits than the first portion nor does Jeddeloh disclose an input register and an output register coupled to the TLB and to the control logic, wherein the control logic is to compare a portion of an initial address in the input register with entries in the TLB and holding a first translated address in the output register. However, Alpert teaches the concept of performing a lookup (functionality parallel to the comparing function above) of a first portion (Figure 2, Reference 46 - page field) of an initial address (Figure 2, Reference 41 - linear address) in a conversion table (C 8, L 45-50 - page table, larger form of a TLB) and combining a first value (page frame address from the page table – refer to Figure 2, Reference 24; Figure 8, Page table entry format) associated with a matching entry (corresponding entry - when a lookup is performed a corresponding entry is found) with a second portion of the initial address (Figure 2, Reference 48 - offset) to form a first translated address (physical address)(C 8, L 48-51 – the physical address comprises the page frame address and the offset), wherein the first value has a greater number of bits than the first portion (Alpert discloses a 32 bit linear address [C 3, L 36-40; C 4, L 33-35] comprising a 2 bit pointer field [Figure 2, Reference 42; C 10, L 51-53], a 9 bit directory field [Figure 2, Reference 44; C 10, L 60-61], a 9 bit page field [Figure 2, Reference 46; C 10, L 66-67; C 11, L 1-2] and an offset field comprised of the remaining 12 bits [Figure 2, Reference 48]; the first value, [page frame number], comprises 24 bits, [refer to Figure 8, page table entry format, page frame

address] and the first portion, [page field], of the initial address comprises 9 bits; thus the first value has a greater number of bits than the first portion). This feature taught by Alpert expands the addressing capability of an architecture with a limited addressing range, such as the system taught by Porterfield, by mapping/translating the virtual/linear addresses to larger physical addresses. The width of the physical address is extended thereby allowing the system to access memory beyond its capabilities based upon the width of the virtual/linear address. Additionally, Dixit teaches a TLB (Figure 1, comprised of references 12, 14, 16, 20, 22, 24, 28, 30, 31, 32 and 34) coupled to an input register (Figure 18; C 3, L 12-14) and an output register (Figure 1, Reference 26; C 3, L 20) and control logic (software or hardware logic for controlling the operation of the TLB), wherein the control logic is to compare an initial address in the input register with the entries in the TLB and wherein a translated address is held in the output register (C 3, L 9-22). It is well known in the art to store data/addresses in a register for the purpose of reducing jitter and glitches from the signals thereby providing accurate and stable data outputs. Jeddeloh addresses are not disclosed as stored in registers and thus are vulnerable to the effects of glitches and jitter. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings of Alpert and Dixit with the teachings of Jeddeloh for the desirable purpose of expanding the address capability of a system by allowing the system to access a larger amount of physical memory and thereby improving the performance of the system and for the desirable purpose of providing stability and accuracy.

Regarding claim 16, Jeddeloh, Alpert and Dixit disclose the control logic is further configured to access a table (comprehensive table) in memory if the matching entry is not found (Jeddeloh - C

6, L 30-34; C 7, L 12-15), find a second value (physical page/frame number) in the table associated with the first portion, combine the second value with the second portion to form a second translated address (Jeddeloh - Figure 3, References 310, 312 - the second value and the offset of the initial address are combined to perform a memory operation and are thus combined to form a physical address) and hold the second translated address in the output register (Dixit - C 3, L 18-22).

Regarding claim 17, Jeddeloh, Alpert and Dixit disclose the control logic including logic for first and second control flows, wherein the second control flow is to translate an initial graphics controller address and does not access the table (Jeddeloh – C 7, L 9-12; the control logic responsible for translating an address using the GART, when a GART hit occurs) and wherein the first control flow is to translate an initial bus controller address and accesses the table (Jeddeloh – C 7, L 12- 15; the control logic responsible for translating an address using the comprehensive table in system memory – when a GART miss occurs).

Claim 18 is rejected for the same rationale applied to claim 15 above with regard to the first value having a greater number of bits than the first portion.

7. Claims 23-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (USPN: 6,477,623) in view of Alpert et al. (USPN: 5,802,605) .

Regarding claim 23, Jeddeloh discloses reading a first address (Figure 3, Reference 302- a received address is read from an input such as a bus, signal line, etc.) containing a first number

of bits (length of the virtual address) and having an upper portion (virtual/linear address excluding the offset) and a lower portion (offset portion of the virtual/linear address); comparing the upper portion with a plurality of entries in a first table (GART table) and if the upper portion matches a particular one of the plurality of first entries, selecting a second entry (physical page number/address) in the first table associated with the particular one of the plurality of first entries and combining the second entry with the lower portion to form a first translated address (Figure 3, References 310, 312; C 7, L 9-18 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses (C 6, L 28-30) and thus TLBs function such that a virtual/linear address, [excluding the offset], is compared to the addresses in the TLB and when a match is found, a physical address is formed by combining the physical page number [translated address] with the offset of the virtual/linear address and thus it is evident that these steps are performed when performing steps 310 and 312 in Figure 3) and transmitting the first translated address (Figure 3, Reference 312 - the translated address is transmitted to the memory to perform the memory operation [accessing the memory]). Jeddeloh does not disclose the second entry containing a greater number of bits than the upper portion. However, Alpert teaches the concept of performing a lookup (functionality parallel to the comparing function above) of an upper portion (Figure 2, Reference 46 - page field) of an initial address (Figure 2, Reference 41 - linear address) in a conversion table (C 8, L 45-50 - page table, larger form of a TLB) and selecting and combining a second entry (page frame address from the page table – refer to Figure 2, Reference 24; Figure 8, Page table entry format) associated with a matching entry (corresponding entry - when a lookup is performed a corresponding entry is found) with a lower portion of the first address (Figure 2, Reference 48 - offset) to form a first translated

address (physical address)(C 8, L 48-51 – the physical address comprises the page frame address and the offset) and transmitting the first translated address (the address is transmitted to main memory for access), wherein the second entry has a greater number of bits than the upper portion (Alpert discloses a 32 bit linear address [C 3, L 36-40; C 4, L 33-35] comprising a 2 bit pointer field [Figure 2, Reference 42; C 10, L 51-53], a 9 bit directory field [Figure 2, Reference 44; C 10, L 60-61], a 9 bit page field [Figure 2, Reference 46; C 10, L 66-67; C 11, L 1-2] and an offset field comprised of the remaining 12 bits [Figure 2, Reference 48]; the second entry, [page frame number], comprises 24 bits, [refer to Figure 8, page table entry format, page frame address] and the upper portion, [page field], of the initial address comprises 9 bits; thus the second entry has a greater number of bits than the upper portion). This feature taught by Alpert expands the addressing capability of an architecture with a limited addressing range, such as the system taught by Jeddeloh, by mapping/translating the virtual/linear addresses to larger physical addresses. The width of the physical address is extended thereby allowing the system to access memory beyond its capabilities based upon the width of the virtual/linear address. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings of Alpert with the teachings of Jeddeloh for the desirable purpose of expanding the address capability of a system by allowing the system to access a larger amount of physical memory and thereby improving the performance of the system.

Regarding claims 24 and 26, Jeddeloh and Alpert teach if the upper portion does not match any of the plurality of first entries in the first table accessing a second table (comprehensive table) having a plurality of third entries (physical page/frame number) and indexing the second table

with the upper portion to identify a particular one of the plurality of third entries (Jeddeloh - C 6, L 30-34; C 7, L 12-15; the comprehensive table is indexed to find the translation for the virtual/linear address), combining the particular one of the plurality of third entries with the lower portion to form a second translated address (Jeddeloh - Figure 3, References 310, 312 - the particular one of the plurality of third entries and the offset of the first address are combined to perform a memory operation and are thus combined to form a physical address for accessing the memory) and transmitting the second translated address to the memory via the memory interface logic (memory controller) internal to the input-output controller (Figure 3, Reference 312 - the translated address is transmitted to the memory, via memory controller [Reference 104, Figure 1; C 3, L 35-38] to perform the memory operation [accessing the memory]).

Regarding claim 25, Jeddeloh and Alpert disclose the first table contained in an input-output controller (Jeddeloh - the GART table is contained within input-output controller [Reference 102, Figure 2]) and the second table is contained in main memory (Jeddeloh - C 6, L 30-34; C 7, L 12-15 - the comprehensive table is contained in system memory).

Regarding claim 27, Jeddeloh and Alpert disclose the first table as a translation lookaside buffer (Jeddeloh - Figure 2, Reference 202 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses [C 6, L 28-30]).

Regarding claim 28, Jeddeloh and Alpert disclose reading a first address from a bus controller (Jeddeloh – C 6, L 36-50; Jeddeloh discloses that addresses are received from any of the elements coupled to switch, Reference 124 in Figure 2);

Regarding claim 29, Jeddeloh and Alpert disclose the first table used to translate addresses from a graphics controller (Jeddeloh – C 6, L 17-50).

8. Claims 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (USPN: 6,477,623) in view of Alpert et al. (USPN: 5,802,605).

Regarding claim 30, Jeddeloh discloses an address translator (Figure 2, comprised of References, 124 and 202, [the translation table stored in GART]) having a first interface to couple to a memory controller (signal line(s) within Reference 124 coupled to Reference 122), a second interface to couple to a graphics controller (signal line(s) within Reference 124 coupled to Reference 140), a third interface to couple to a bus controller (signal line(s) within Reference 124 coupled to Reference 130) and a table of entries, each entry having a first portion and a second portion (Figure 2, Reference 202; table stored within GART); a translation control circuit coupled to the address translator to program the entries in the address translator (the address translator comprises interfaces and a table, wherein neither of these elements have logic to control the operation of the address translator and thus it is evident that logic is coupled to the address translator for controlling its operations such as storing/programming addresses/entries in the table); wherein the address translator is to translate an address on the third interface into a first address on the first interface and to translate an address on the second interface into a

second address on the first interface (C 6, L 36-50 - Jeddeloh discloses that addresses are received from any of the elements coupled to Reference 124 in Figure 2, and are translated using the table in the GART as long as the address falls within a reserved range of addresses). Jeddeloh does not disclose the address translator translating an address on the third interface into a first address on the first interface having a greater number of bits than the address on the third interface nor translating an address on the second interface into a second address on the first interface having a greater number of bits than the address on the second interface. However, Alpert teaches the concept of an address translator translating an initial address into a first address, wherein the first address has a greater number of bits than the initial address (C 3, L 36-40; C 4, L 33-40; C 7, L 32-41; C 8, L 12-50). This feature taught by Alpert expands the addressing capability of an architecture with a limited addressing range, such as the system taught by Jeddeloh, by mapping/translating the virtual/linear addresses to larger physical addresses. The width of the physical address is extended thereby allowing the system to access memory beyond its capabilities based upon the width of the virtual/linear address. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings of Alpert with the teachings of Jeddeloh for the desirable purpose of expanding the address capability of a system by allowing the system to access a larger amount of physical memory and thereby improving the performance of the system.

Regarding claim 32, Jeddeloh and Alpert disclose the address translator comprising a graphics translation lookaside buffer (Figure 2, Reference 202 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses [C 6, L 28-30]).

Response to Arguments

9. Applicant's arguments with respect to claims filed November 25, 2002 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo can be reached on 703-308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7329 for regular communications and 703-746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

February 9, 2003